Appendix B – Diagrams and Physical Interfaces

(excerpted from WAAS documentation)

WMS Safety Computer Block Diagram 3

GUST Safety Computer Block Diagram 4

Comparator Board Logic Diagram 5

Safety Computer Chassis - Front Panel 8

Safety Computer Chassis - Rear Panel 9

WMS Safety Computer Block Diagram

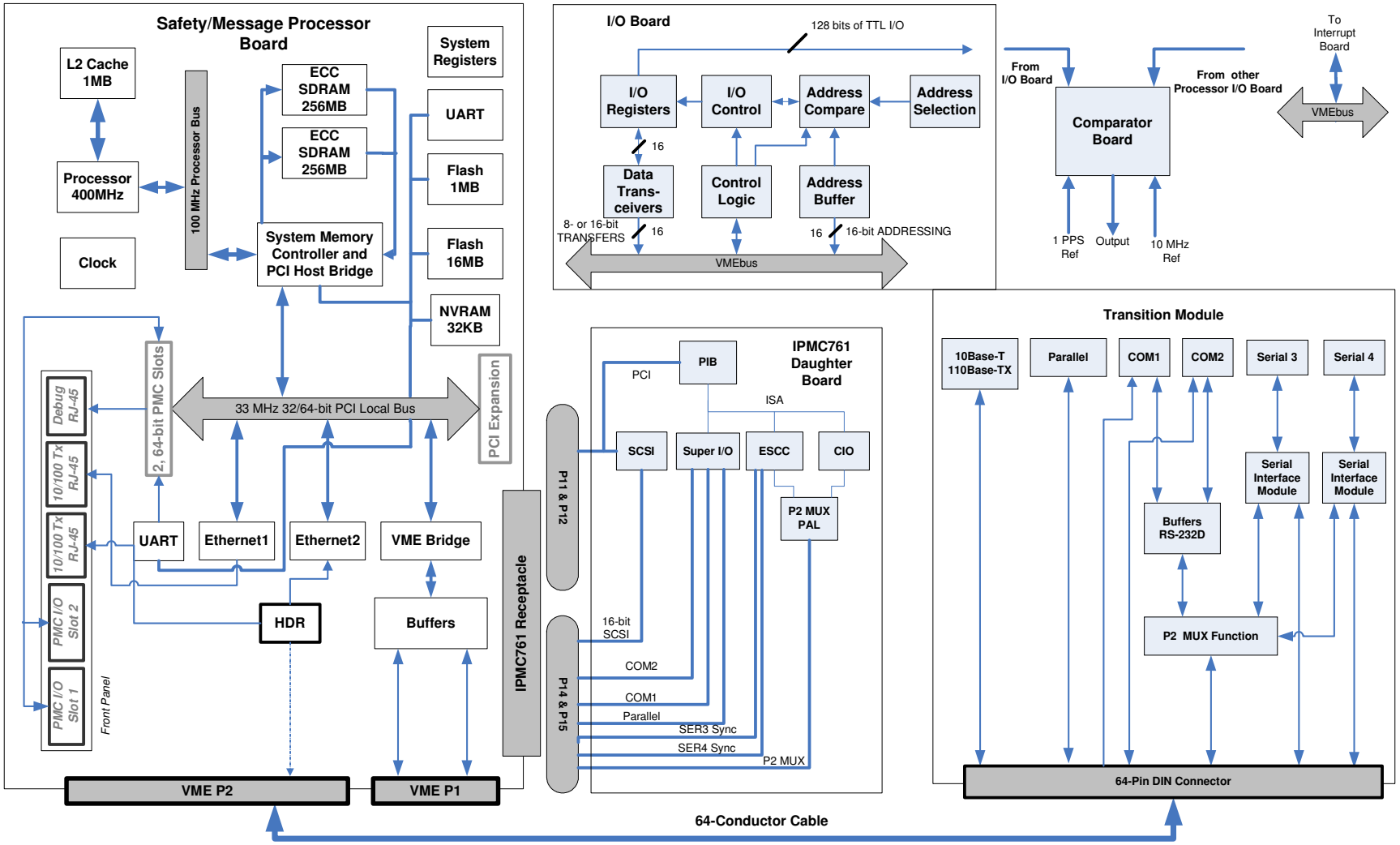


Figure 1. WMS Safety Computer Block Diagram

GUST Safety Computer Block Diagram

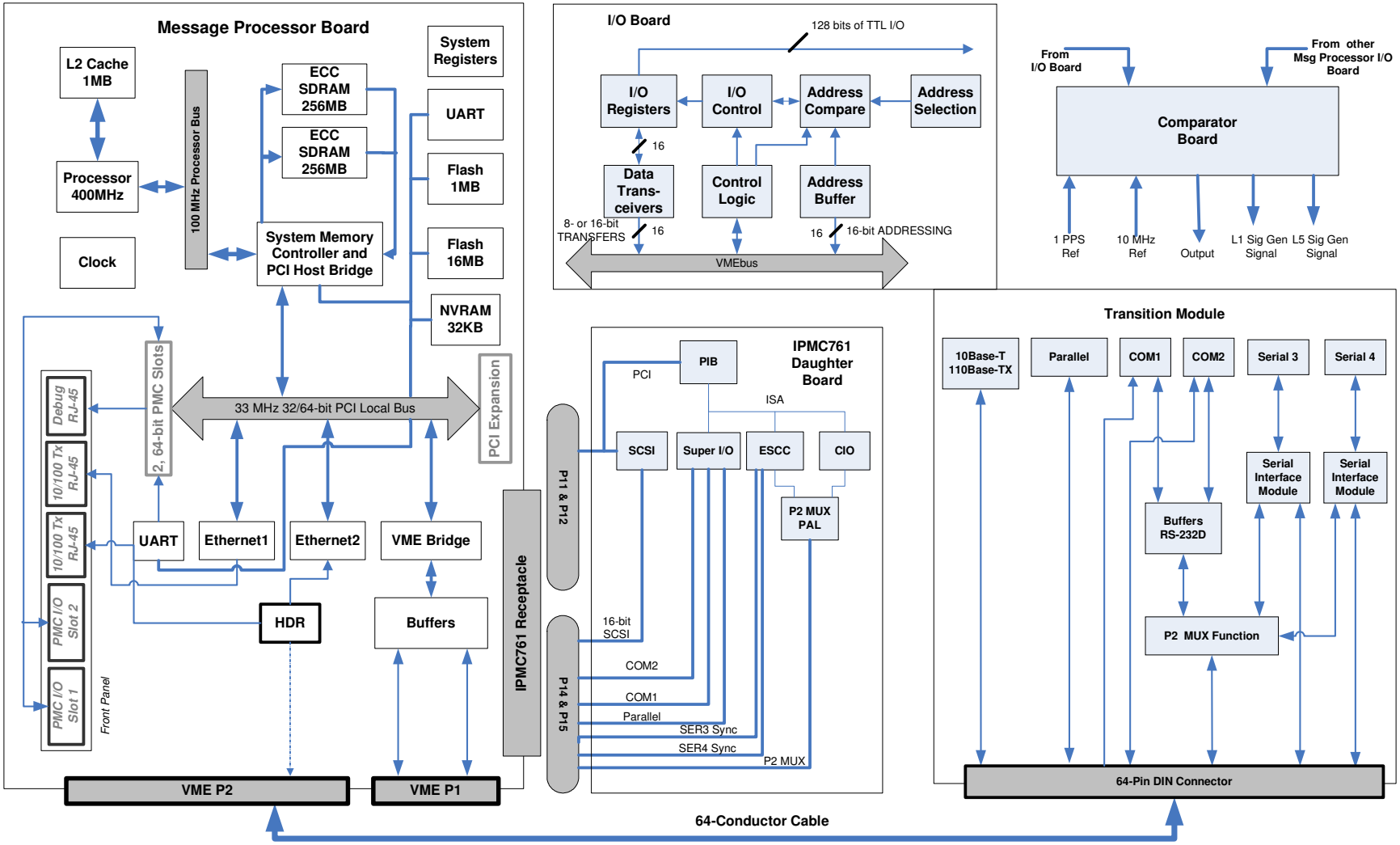


Figure 2. GUST Safety Computer Block Diagram

Comparator Board Logic Diagram

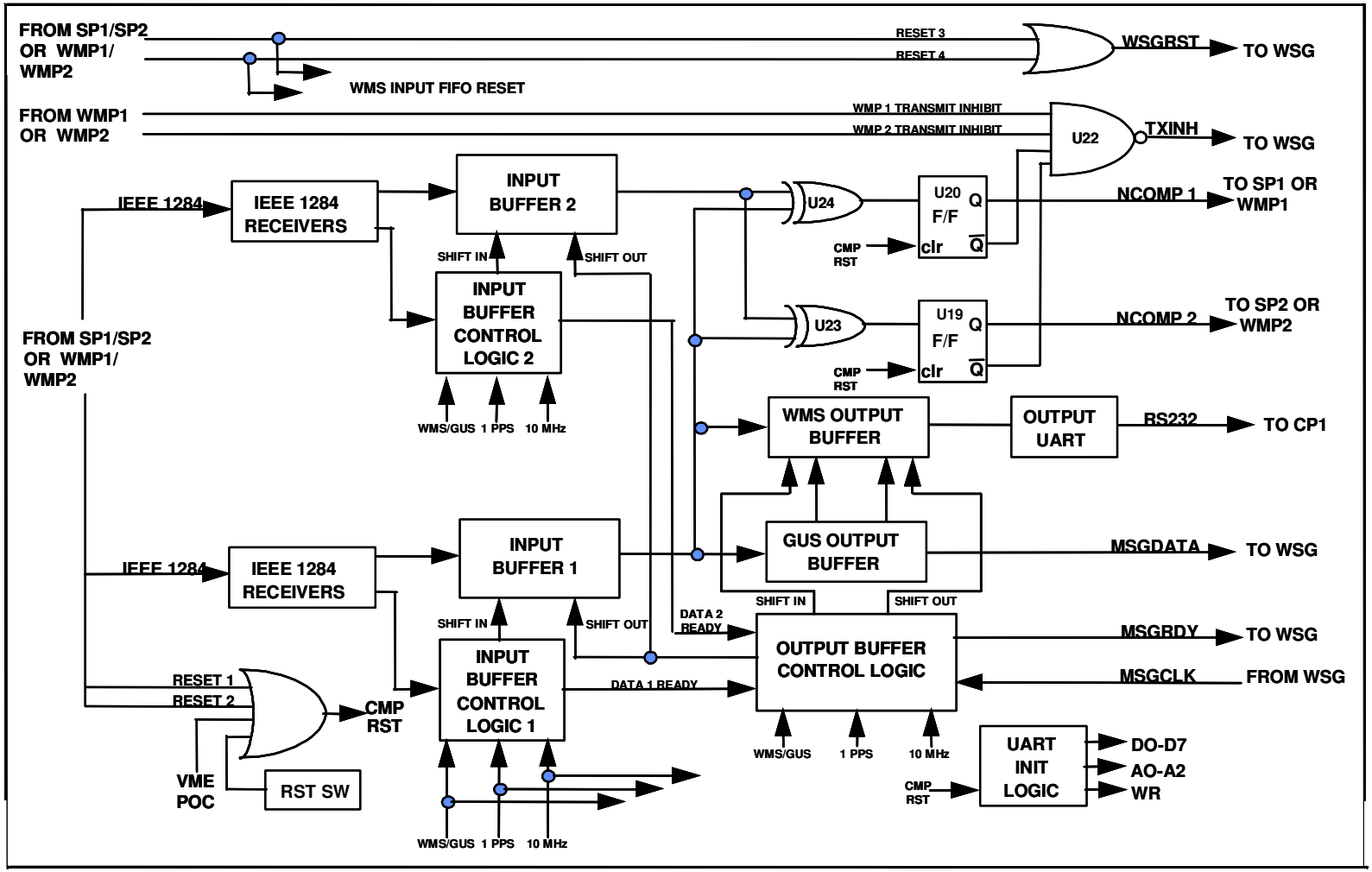


Figure 2. Sample Comparator Logic Diagram

Each message processor (with I/O module) contains the following items:

- MPC7400 microprocessor @ 400-MHz internal clock frequency.
- L2 cache, 1MB using burst mode SRAM
- Main Memory - 512 MB PC100 ECC SDRAM with 100 MHz bus on board.
- 32 KB NVRAM
- Flash memory, EEPROM, on-board programmable 1MB via two 32-pin PLCC sockets; 16 MB surface mount
- System Memory Controller
- PCI Host Bridge
- Multi-processor Interrupt Controller
- Dual 16550-Compatible Asynchronous Serial Ports

I/O Module containing: (daughter board mounted on processor via IPMC761 receptacle; refer to block diagram)

- Inter-Integrated circuit capability
- 8-bit Bi-directional full IEEE 1284 Parallel Port Interface
- Two Asynchronous Serial Port Interface capable of supporting EIA-574 DTE, EIA-232, 38.4K BPS, 115K BPS raw.
- Two Asynchronous/Synchronous Serial Port Interfaces
- ISA to PCI Interface.

The Input/Output board includes:

- Interrupts on any of seven levels of the ISO OSI Model
- 128 bits of TTL I/O
- Sixteen 8-bit I/O port selectable I/O operation on 8-bit boundaries
- Port data available for direct read
- 8-bit or 16-bit data transfers
- Four 64-pin DIN-type input connectors

The Comparator includes:

- Reset capability via reset switch on Safety Computer front panel.
- Capability to receive 1 (63 byte) or 2-9 (500 bit) messages from the WAAS Message Processors every second.
- Parallel IEEE 1284 interfaces to the Safety Processors.
- Perform bit-by-bit comparison of all messages from each of the dual WAAS Message Processors.
- Generate two (L1 and L5) transmit inhibit signals (active high) to the Signal Generator Type 1 based on a transmit inhibit signal (active high) from either GCCS Message Processors or upon the detection of a no-compare results.
- Provide two custom RS-232 UART serial interfaces to the Signal Generator type 1 (L1/L5 interfaces)
- Receive and convert 1PPS signal into 0.5 Hz signal to each Message Processor.

- RS-232 UART serial interface to the C&V Processor with a data rate of 115.2 KBPS.

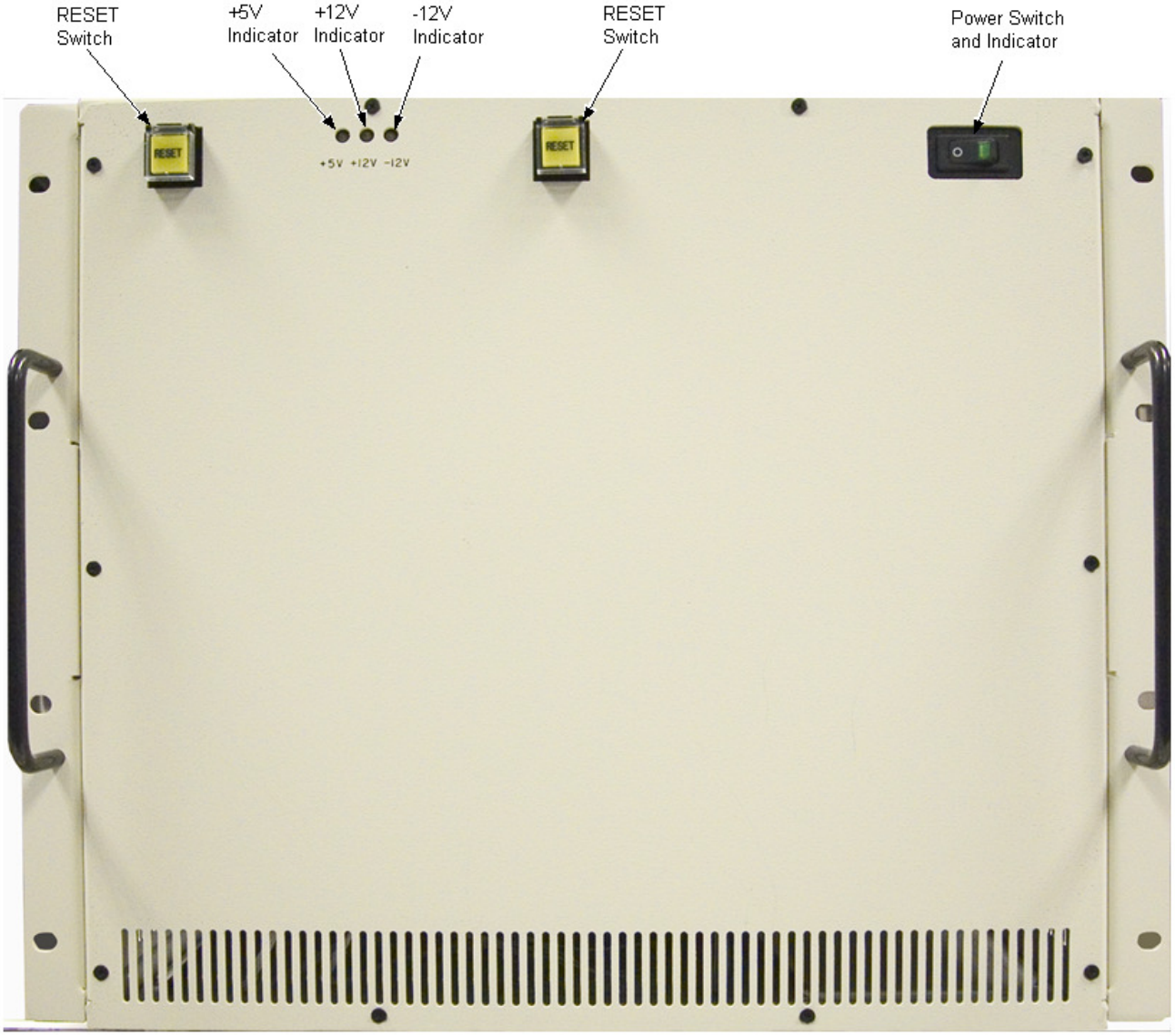
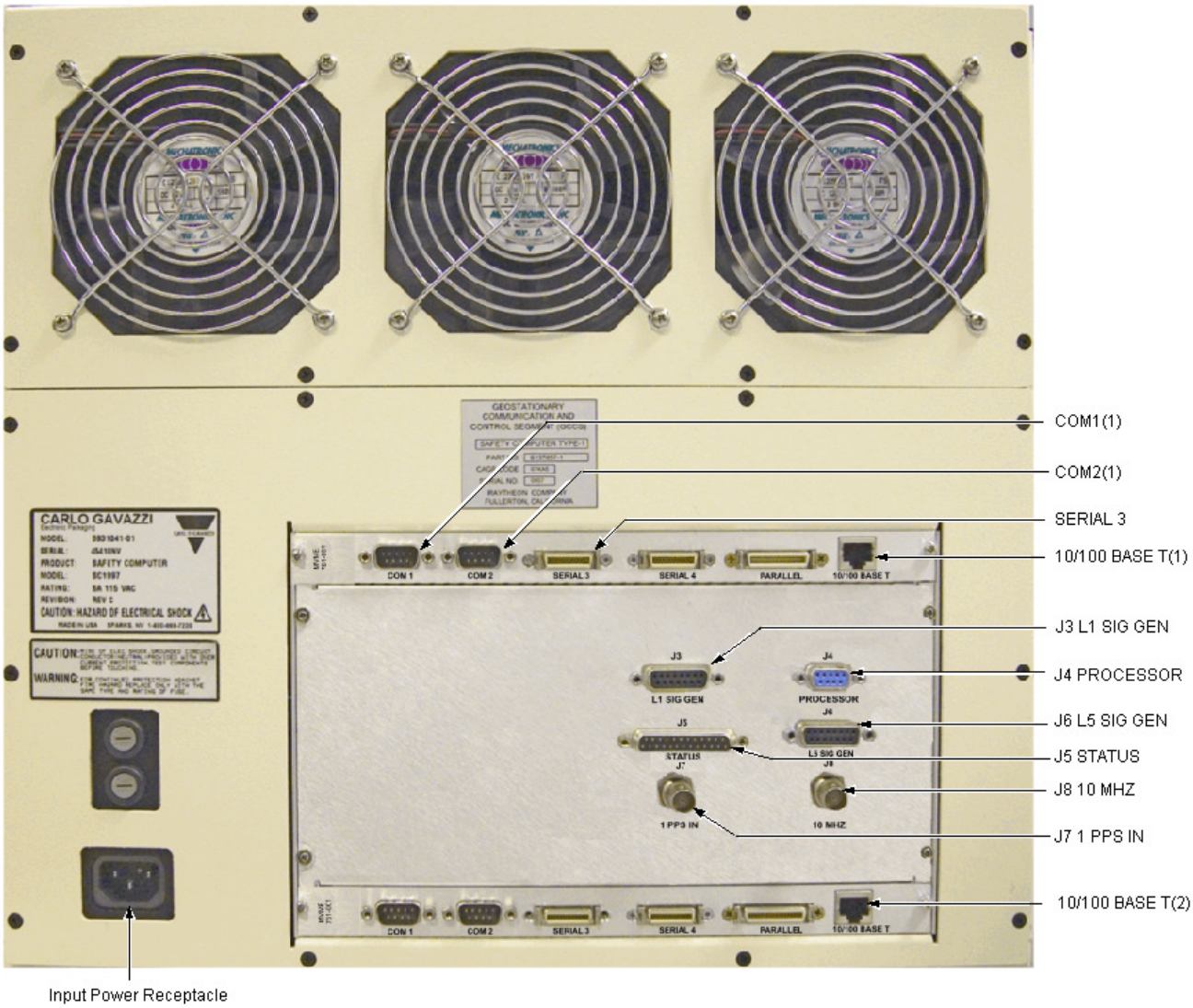
The Transition Module includes:

- 96-pin 3-row DIN P2 Adapter Module and cable (for 8-bit SCSI)
- One HD-36 Parallel Port Connector
- Two DB-9 Asynchronous Serial Port Connectors
- One RJ-45 Ethernet Connector
- Two HD-26 Asynchronous/Synchronous Serial Port Connectors

The Interrupt board includes:

- Four 8-bit ports with each port identified with COS Interrupt Vector
- Interrupts supported by MC68153 Bus Interrupter Module (BIM)
- Interrupts on any of seven levels of the ISO OSI Model
- 8-bit or 16-bit data transfers
- 64-pin DIN type input connector on front panel
- Port data available for direct read

Safety Computer Chassis - Front Panel



Safety Computer Chassis - Rear Panel